I. Listing of Claims

1-4. (Cancelled).

5. (Previously Presented): The field-effect transistor as claimed in claim 9, wherein a gate insulation layer is formed at sidewalls of the gate layer.

6. (Previously Presented): The field-effect transistor as claimed in claim 9, wherein the field-effect transistor is bounded by shallow trench isolations.

7. (Previously Presented): The field-effect transistor as claimed in claim 9, wherein the field-effect transistor has lateral structures < 100 nm.

8. (Previously Presented): The field-effect transistor as claimed in claim 9, wherein the source and drain depressions have a depth of approximately 50 nm to 300 nm.

9. (Previously Presented): A field-effect transistor with local source-drain insulation, having

a semiconductor substrate;

a source depression and a drain depression, which are formed in a manner spaced apart from one another in the semiconductor substrate, wherein the

source and drain depressions have, in an upper region, a widening with a predetermined depth for realizing defined channel connection regions;

a depression insulation layer, which is formed at least in a bottom region of the source depression and of the drain depression, wherein the depression insulation layer has a depression sidewall insulation layer, which is formed in a sidewall region of the source and drain depressions but does not touch the gate dielectric; and

an electrically conductive filling layer, which is formed for realizing source and drain regions and for filling the source and drain depressions at a surface of the depression insulation layer, wherein the electrically conductive filling layer has a seed layer for improving a deposition in the source and drain depressions, the seed layer comprising silicon or SiGe;

a gate dielectric, which is formed at a substrate surface between the source and drain depressions; and

a gate layer, which is formed at a surface of the gate dielectric,

wherein the depression sidewall insulation layer extends into a region below the gate dielectric and overlaps with the gate and the gate dielectric.

10-24 (Cancelled).

25. (New): The field effect transistor as claimed in claim 9, wherein the source and drain depressions form a step at the widening.

26. (New): The field effect transistor as claimed in claim 9, wherein the widening is filled with a first material different from a second material of the seed layer.